Please amend 8/2/04

AMENDMENTS TO THE CLAIMS

Please amend claims 1, 5, 6, 10, and 14, and cancel claims 19 and 20 without prejudice, such that the status of the claims is as follows:

1. (Currently amended) A differential amplifier circuit for amplifying an input signal and for providing an output signal representative of the input signal, the differential amplifier circuit comprising:

first and second input signal nodes;

a first amplifier circuit including an input transistor operatively connected to the first input signal node;

a second amplifier circuit including an input transistor operatively connected to the second input signal node;

a first coupling circuit including a capacitor and ~~an active element~~ a coupling transistor, the first coupling circuit being connected such that ~~the capacitor and the active element are coupled in series between~~ a base of the coupling transistor is connected to the first input signal node and the capacitor is connected between an emitter of the coupling transistor and a base of the input transistor of the second amplifier circuit; and

a second coupling circuit including a capacitor and ~~an active element~~ a coupling transistor, the second coupling circuit being connected such that ~~the capacitor and the active element are coupled in series between~~ a base of the coupling transistor is connected to the second input signal node and the capacitor is connected between an emitter of the coupling transistor and a base of the input transistor of the first amplifier circuit.

2. (Previously presented) The differential amplifier circuit of claim 1 wherein the input transistors of the first and second amplifier circuits each have a base, a collector and an emitter, and the first and second amplifier circuits each include:

a collector circuit connected between a fixed potential and the collector of the input transistor; and

a current generator for directing current through the input transistor and the collector circuit.

3. (Original) The differential amplifier circuit of claim 2 wherein the collector circuit of each of the amplifier circuits includes a cascode stage.

4. (Original) The differential amplifier circuit of claim 3 wherein the cascode stage of each of the amplifier circuits comprises:

a cascode transistor having a base, a collector, and an emitter, wherein the base is connected to a bias potential, and the emitter is connected to the collector of the input transistor of the respective amplifier circuit; and

a resistor connected between the fixed potential and the collector of the cascode transistor.

5. (Currently amended) The differential amplifier circuit of claim 1 wherein each of the first and second coupling circuits ~~each~~ further comprises:

~~a transistor having a base, a collector, and an emitter, wherein the base is connected to the corresponding input signal node, and the collector is connected to a fixed potential;~~

~~a capacitor connected between the emitter of the transistor and the base of the input transistor of the corresponding amplifier circuit; and~~

a current generator for directing current through ~~the~~ a respective coupling transistor.

6. (Currently amended) A read system for reading information from a magnetic storage medium using a magnetoresistive head and for providing an output signal representative of the information read, the read system comprising:

first and second input signal nodes for connection to the magnetoresistive head;

a first amplifier circuit including an input transistor operatively connected to the first input signal node;

a second amplifier circuit including an input transistor operatively connected to the second input signal node;

a first coupling circuit including a capacitor and ~~an active element~~ a coupling transistor, the first coupling circuit being connected such that ~~the capacitor and the active element are coupled in series between~~ a base of the coupling transistor is connected to the first input signal node and the capacitor is connected between an emitter of the coupling transistor and a base of the input transistor of the second amplifier circuit; and

a second coupling circuit including a capacitor and ~~an active element~~ a coupling transistor, the second coupling circuit being connected such that ~~the capacitor and the active element are coupled in series between~~ a base of the coupling transistor is connected to the second input signal node and the capacitor is connected between an emitter of the coupling transistor and a base of the input transistor of the first amplifier circuit.

7. (Previously presented) The read system of claim 6 wherein the input transistors of the first and second amplifier circuits each have a base, a collector and an emitter, and the first and second amplifier circuits each include:

a collector circuit connected between a fixed potential and the collector of the input transistor; and

a current generator for directing current through the input transistor and the collector circuit.

8. (Original) The read system of claim 7 wherein the collector circuit of each of the amplifier circuits includes a cascode stage.

9. (Original) The read system of claim 8 wherein the cascode stage of each of the amplifier circuits comprises:

a cascode transistor having a base, a collector, and an emitter, wherein the base is connected to a bias potential, and the emitter is connected to the collector of the input transistor of the respective amplifier circuit; and

a resistor connected between the fixed potential and the collector of the cascode transistor.

10. (Currently amended) The read system of claim 6 wherein each of the first and second coupling circuits ~~each~~ further comprises:

~~a transistor having a base, a collector, and an emitter, wherein the base is connected to the corresponding input signal node, and the collector is connected to a fixed potential;~~

~~a capacitor connected between the emitter of the transistor and the base of the input transistor of the corresponding amplifier circuit; and~~

a current generator for directing current through ~~the~~ a respective coupling transistor.

11. (Previously presented) In a read system that includes first and second input signal nodes for connection to a magnetoresistive head, that includes first and second input transistors, and that includes first and second collector circuits connected between a fixed potential and the respective first and second input transistors, the improvement comprising:

a first coupling circuit comprising a first coupling transistor having a base connected to the first input signal node, a collector connected to the fixed potential, and an emitter ac coupled to a base of the second input transistor, and a current generator for directing current through the first coupling transistor; and

a second coupling circuit comprising a second coupling transistor having a base connected to the second input signal node, a collector connected to the fixed potential, and an emitter ac coupled to a base of the first input transistor, and a current generator for directing current through the second coupling transistor.

12. (Previously presented) The read system of claim 11 wherein a first capacitor is connected between the emitter of the first coupling transistor and the base of the second input transistor, and a second capacitor is connected between the emitter of the second coupling transistor and the base of the first input transistor.

13. (Original) A read system for reading information from a magnetic storage medium using a magnetoresistive head and for providing an output signal representative of the information read, the read system comprising:

first and second input signal nodes for connection to the magnetoresistive head;

a first transistor having a base, a collector, and an emitter, wherein the emitter is connected to the first input signal node;

a second transistor having a base, a collector, and an emitter, wherein the emitter is connected to the second input signal node;

a third transistor having a base, a collector, and an emitter, wherein the emitter is connected the collector of the first transistor, and the base is connected to a bias potential;

a fourth transistor having a base, a collector, and an emitter, wherein the emitter is connected the collector of the second transistor, and the base is connected to the bias potential;

a first resistor connected between the collector of the third transistor and a first fixed potential;

a second resistor connected between the collector of the fourth transistor and the first fixed potential;

a first current generator connected between the emitter of the first transistor and a second fixed potential;

a second current generator connected between the emitter of the second transistor and the second fixed potential;

a fifth transistor having a base, a collector, and an emitter, wherein the base is connected to the second input signal node, and the collector is connected to the first fixed potential;

a sixth transistor having a base, a collector, and an emitter, wherein the base is connected to the first input signal node, and the collector is connected to the first fixed potential;

a first capacitor connected between the emitter of the fifth transistor and the base of the first transistor;

a second capacitor connected between the emitter of the sixth transistor and the base of the second transistor;

a third current generator connected between the emitter of the fifth transistor and the second fixed potential; and

a fourth current generator connected between the emitter of the sixth transistor and the second fixed potential.

14. (Currently amended) A method of amplifying an input signal from a magnetoresistive head, the input signal comprising a differential signal including a first signal provided at a first input signal node and a second signal provided at a second input signal node, the first and second input signal nodes being connected to opposite sides of the magnetoresistive head, the method comprising:

amplifying the first signal with a first amplifier circuit that includes a first input transistor to provide an amplified first signal;

amplifying the second signal with a second amplifier circuit that includes a second input transistor to provide an amplified second signal;

coupling a first capacitor and a first ~~active element~~ coupling transistor ~~in series~~ between the first input signal node and a base of the second input transistor such that a base of the first coupling transistor is connected to the first input signal node and the first capacitor is connected between an emitter of the coupling transistor and the base of the second input transistor; and

coupling a second capacitor and a second ~~active element~~ coupling transistor ~~in series~~ between the second input signal node and a base of the first input transistor such that a base of the second coupling transistor is connected to the second input signal node and the second capacitor is connected between an emitter of the coupling transistor and the base of the first input transistor.

15. (Previously presented) The method of claim 14, wherein the step of amplifying the first signal with the first amplifier circuit comprises:

coupling the first input transistor to the first input signal node;

coupling a first cascode transistor to the first input transistor; and

coupling a first resistor to the first cascode transistor, the amplified first signal being provided between the first resistor and the first cascode transistor.

16. (Previously presented) The method of claim 15, wherein the step of amplifying the second signal with the second amplifier circuit comprises:

coupling the second input transistor to the second input signal node;

coupling a second cascode transistor to the second input transistor; and

coupling a second resistor to the second cascode transistor, the amplified second signal being provided between the second resistor and the second cascode transistor.

17-20. (Canceled)